LOW POWER AND HIGH SPEED PARALLEL TEST ACCESS MECHANISM USING MAJORITY LOGIC TECHNIQUE

P.ANUSUYA
PG SCHOLAR
Jayaram College of Engineering & Technology
Trichy, India
anusuyaabirami@gmail.com

A.KAVITHA
PROFESSOR
Jayaram College of Engineering & Technology
Trichy, India
susmi_sri@yahoo.com

***Abstract*-- A test-access architecture also referred to as a test-access mechanism (TAM) provides the means for on-chip test data transport. Now a days, multi core processor consists of more no of complex digital architecture. This architecture consumes more circuit area and power. This type of core processor used in many applications and improves the performance level. But it has some problem due to circuit complexity level. It causes more error in the internal core architecture output results. In the proposed approach, test access mechanism provides the mean for on-chip test data transport along with detection of faults. This method is to design the low-power scan chain based parallel multi core testing architecture using majority logic technique. This technique used to test all the internal core architecture in parallel form and to identify the faulty circuit. These works implements the test pattern creation and apply the scan chain process. This process analyze the separate core internal architecture output result values. Finally, it improves the system performance and reduces the power consumption level. This paper demonstrates the simulation results for the generation of test patterns and compression of test patterns. Also it involves the detection of faults. Xilinx software tool is used for the verification of results.**

Key words: Test Access Mechanism, Majority Logic Technique, Multi-Core Architecture.

I. INTRODUCTION

A. System-On-Chip:

System-on-chip (SOC) is designed based on reusable intellectual property (IP) cores. SOCs can reduce manufacture cost and offer rapid system implementation. However, the testing for SOC has become a significant and serious challenge. To simplify complexity of test access and application the modular test of the IP cores in an SOC is utilized frequently. In modular test, core test wrapper isolates an embedded core from its environment, and test access mechanism (TAM) which facilitates modular testing is developed to transport test data from the SOC pins to core terminals. SOC test techniques requires specialized hardware infrastructure such as TAM and test wrappers.

B. CUT with DFT Function

Our circuit under test function is considering the different arithmetical core architecture. These architectures are produce the 16 bit output result in each process. Circuit under test was performed before the device assembly. The results in prevention of circuit and device and also the fault detected at this stage results less cost than the fault identified at device level. Our work is to identify the faulty circuit effectively and separately in multi core architecture. This architecture is to modify the testing methodology using majority logic function.

C. Testing of Product

System testing is the stage of implementation, which aimed at ensuring that system works accurately and efficiently before the live operation commence. Testing is the process of executing a program with the intent of finding an error. A good test case is one that has a high probability of finding an error. A successful test is one that answers a yet undiscovered error. System testing makes a logical assumption that if all parts of the system are correct, the goal will be successfully achieved. The candidate system is subject to variety of tests-on-line response, recovery and security and usability test. A series of tests are performed before the system is ready for the user acceptance testing.

D. Test Access Mechanism:

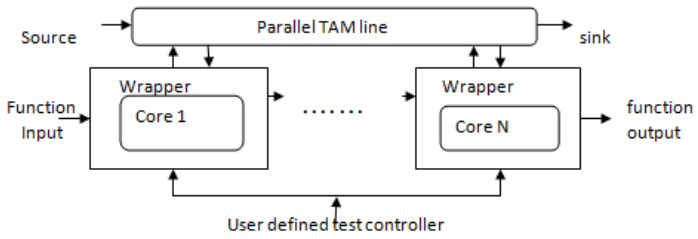

Fig 1. Testing of SOC using TAM

Many system-on-chip (SoC) integrated circuits today contain multiple hierarchy levels for both design and test. TAM technique avoids wasting excess free variables and improves the compression ratio of SOC testing. Consequently, it can help with controlling the SOC test cost. TAM technique is applied to deliver test vectors from the source to CUT.

The main function of TAM is to transport test responses from the CUT to the test sink. TAM design involves making tradeoff, data transport capacity, test time and TAM overhead. Cores using the same TAM lines are tested sequentially unless their test patterns are compatible, while those using the different TAM lines can be tested in parallel. Compressed

test data is delivered from tester via TAM to linear decompressor in the cores. Then the test patterns decompressed by linear decompressor are shifted into scan chains in cores. To guarantee the compressibility of each test cubes for a single core, the number of free variables of the linear decompressor should be set according to the largest number of care bits in a test cube. We present two approaches for efficient testing of SoCs with hierarchical cores. In the first approach, a conventional wrapper design is used which gives flexibility for TAM optimization and test scheduling. In the second approach, for testing of parent and child cores a modified wrapper design is used. This achievement can be attributed to advances in semiconductor process technology and it provides high performance, low power, and short time-to-market.

II. RELATED WORK

A novel method for statistically encoding test vectors for full-scan circuits using selective Huffman coding is presented in [7]. The deterministic test vector compression technique for SoCs using block matching has been presented in [1].A scheme for compression and decompression of test data using cyclical scan chain is presented in [2]. A professional approach for compressing test data using run-length coding and Burrows–Wheeler transformation (BWT) is existing in [3]. The BIST scheme for non scan circuits based on statistical coding using comma codes and run-length coding is described in Iyengar *et al.* [4]. A test data compression technique using dictionary-based and bitmask selection criteria was proposed by Basu and Mishra [5]. The bitmask-based compression technique [5] is developed to deal with the mismatch problem of the dictionary-based technique by generating more matching patterns. But, the procedure is unable to handle the data set containing don't caare values. A different technique for test data compression/ decompression has been proposed in [6]. It has achieved higher level of compression but it needs extra on-chip hardware and extreme power consumption and time. The author in [8] describes a new approach towards dependable design of homogeneous multi-processor SoCs in an example satellite-navigation application. It has the advantage of fast electronic fault detection/diagnosis and repair. [9] provide an analytical model that covers not only cores but also routers and interconnects. Different fault tolerance approaches such as Forward Error Control (FEC), Automatic Repeat Query (ARQ), and multi-path routing have been used. [10] This paper will compare and contrast both digital and analogue implementations without considering the deep system design of these arrays. It has the advantages of flexible in design, configuration, and application, making it an attractive solution to reduce test time when testing multiple identical cores. The increased use of multicore chips diminishes per-core complexity and also demands parallel design and test technologies. [11] This introduces a novel test access mechanism (TAM) technique for parallel testing of multiple identical cores and identifying faulty cores.

III. PROPOSED SYSTEM

This technique is used to test the all internal core architecture in parallel form. This work is to implement the test pattern creation and to apply the scan chain process. This process is to analysis the separate core internal architecture output result values and fault identification comparison process between expected test response and present test response results. The cores using the exact same TAM lines are divided into a group. Cores in the same group are tested sequentially unless their test patterns are compatible. Those using not identical TAM lines can be tested in parallel. Compressed test data is delivered from tester via TAM and decompressed in the cores by linear decompressor. Then the decompressed test patterns are scanned into scan chains in cores. The developed scheme requires minimum hardware overhead based on on-chip embedded processor can be reused for normal operation The advantage of this system is to improve the TAM system performance level and reduce the power consumption level. It is used to increase the test pattern generation process and reduce overall circuit complexity level. It provides high reliability.

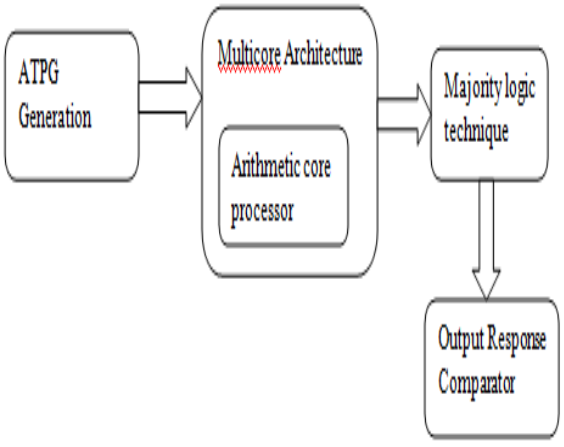

Fig 2. Block diagram of Proposed method

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A lot of schemes used in both TAMs and test wrappers have been proposed towards optimal test application time, test interface architecture, power consumption, control logic,

routing and layout optimization or embedded cores hierarchy. Test data volumes are growing especially for delay test as the VLSI complexity increases. Recently, there is a growing interest in test data compression of SOC testing. ATE delivers test data in a compressed form, and on-chip decompressors expand them into the actual test patterns which will be transported into scan chains. In recent years, SOC test compression schemes based on linear decompression which can provide higher compression ratios continue to appear. The expenses including control data, hardware logic needed in the scheme may adversely prohibit its application. The scheme utilizes a single linear decompressor to expand the tester channels to numerous TAM lines.

They allow multiple cores to be tested simultaneously and allocate tester channels dynamically to decompressors as needed. The proposed SOC test compression approach aims to improve encoding efficiency of linear decompressors. Encoding efficiency is defined as the ratio of the number of care bits in the test cubes to the number of free variables (i.e., the number of compressed bits stored on the tester). The main idea is that the cores tested simultaneously share part of free variables. This scheme avoids wasting excess free variables and improves the compression ratio of SOC testing. Consequently, it can help with controlling the SOC test cost. Conventional SOC test bus architecture with fixed-width is shown. In the architecture the total TAM width is partitioned among several test buses with fixed-width. Cores using the same TAM lines are tested sequentially unless their test patterns are compatible, while those using the different TAM lines can be tested in parallel. Compressed test data is delivered from tester via TAM to linear decompressor in the cores.

MODULE DESCRIPTION

A. ATPG GENERATION

This work is mainly based on automatic different core testing process using reset and clocking sequence. The pseudo random pattern generation process is mainly used to generate the pattern results based on normalized Euclidean distance. LFSR consist of D-FF connected in cascade with the same clock applied to the entire FF to make them act like a shift register. This XOR operation introduces a new bit into the shift register. ATPG (Automatic Test Pattern Generation /Generator) is an electronic design automation technology used to find an input sequence that applied to a digital circuit and it enables automatic test equipment to distinguish between behavior of the correct circuit and the faulty circuit. These patterns are used to test semiconductor devices after manufacture, and in some cases to assist by determining the failure analysis. These metrics generally indicate test quality and test application time.

B. MUTICORE ARCHITECTURE

Our process considers the arithmetic core architecture. It consists of adder, comparator, subtractor, multiplier architecture. This architecture consists of more number of gate components, so it has more chance to error occurs in output results. So every time we analysis the circuit activation process and to detect the error occurrence in multi core architecture.

C. MAJORITY LOGIC TECHNIQUE:

The 16- bit majority architecture is used for the data encoding process and to modify the majority function using the BOOLEAN logic function. It is used to reduce the gate component for the 16-bit majority architecture. This majority architecture optimizes the overall multi core circuit testing process and to improve the system accuracy level.

E. OUTPUT RESPONSE COMPARATOR

The final output is to identify the faulty circuit and also to reduce the test processing time. The output response comparator compares the golden signature from ROM memory and present signature level and provides the result. This proposed majority based multi core circuit scheme is to identify the fault effectively and to reduce the power consumption level during testing.

IV. PERFORMANCE ANALYSIS

Xilinx ISE[1] (Integrated Software Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs which enable us to compile the designs, perform timing analysis, examine RTL diagrams, simulate a different stimuli, and configure the target device with the programmer. To get fine result this technique is implemented in VHDL language.

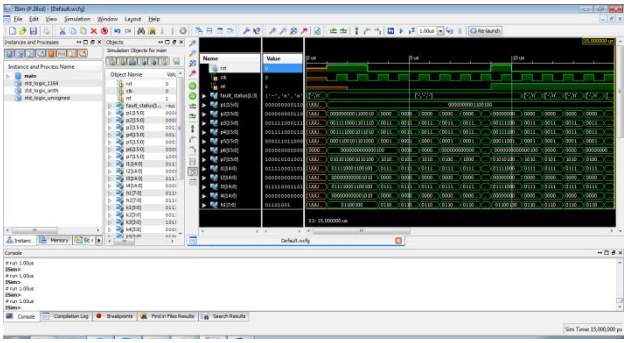

Fig 3. Testvector compression result

The performance is analyzed using RST and CLK signal. The initialization is performed by making RST high, using natural clock at time

1000ns. The resultant output is stored in normal mode. At the same time by making RST low the result is saved in test mode. Making reset high in normal mode the compressed test vector is obtained as an output using majority logic technique. To check the fault detection stuck at fault is introduced. Further fault detection process is carried out by comparing golden signature and present signature.

Fig 4. Power Report.

It shows the power report of this process. In this it consumes 27mW power and 26.2C as junction temperature.

TABLE I
COMPARISON TABLE

PARAMETERS	EXISTING SYSTEM	PROPOSED SYSTEM
Delay Time (ns)	4.923	1.916
Clock Frequency (MHz)	203.1	521.800
Latency Time (ns)	1.764	1.49
Power (mW)	28	27
Slices Count	145	103
LUT'S Count	433	313
Flip-Flop's Count	445	339

V. CONCLUSION

Finally we design the low-power scan chain based parallel multi core testing architecture. This architecture consists of different internal core architecture and the faulty circuit is identified using majority logic technique. The aggressive shrinking of characteristic size and rapid increase of the integrated degree in the electronics industry will bring forward higher requirement on SOC design and test procedures. By sharing free variables between cores tested simultaneously in SOC, the proposed SOC test technique provides greater flexibility in test compression. It does not have detrimental effects on an additional area and potential performance overhead. Experimental results on several larger SOC designs demonstrate the efficiency of the proposed technique. The proposed scheme can also be expanded by sharing common channels among three or more core groups to obtain better results. Meanwhile, the proposed approach can be combined with other approaches, such as test scheduling, to reach higher efficiency.

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